Index	Hermes name	Hermes C3 FPGA pin	HF2 Name	TX2 Name	CVA9 J2 pin	CVA9 name	CVA9 CV FPGA pin	Description
1	_122MHz	150	122_88MHZ	-	5	EG_P1	W16	122.88 MHz input from VCXO
2	OSC_10MHZ	89	EXT_OSC_10MHZ	-	6	EG_P35	N9	10MHz reference input clock
3	FPGA_PLL	144	VCXO_CTL	-	65	EG_P28	U22	VCXO control voltage PWM output
4	ATTN_DATA	39	SPI_DATA	SPI_DATA	62*	EG_P58	V20	data output to attenuator
5	ATTN_CLK	22	SPI_CLK	SPI_CLK	64*	EG_P59	U20	clock output to attenuator
6	ATTN_LE	69	ATTN_LE	-	66	EG_P60	P18	latch enable output to attenuator
7	INA0	187	INA0	-	9	EG_P3	AA13	input data from ADC
8	INA1	186	INA1	-	11	EG_P4	AA14	input data from ADC
9	INA2	185	INA2	-	13	EG_P5	Y14	input data from ADC
10	INA3	184	INA3	-	15	EG_P6	AB15	input data from ADC
11	INA4	183	INA4	-	17	EG_P7	AA15	input data from ADC
12	INA5	177	INA5	-	19	EG_P8	Y15	input data from ADC
13	INA6	176	INA6	-	23	EG_P9	Y16	input data from ADC
14	INA7	173	INA7	-	25	EG_P10	AB17	input data from ADC
15	INA8	171	INA8	-	27	EG_P11	AA17	input data from ADC
16	INA9	169	INA9	-	29	EG_P12	Y17	input data from ADC
17	INA10	166	INA10	-	31	EG_P13	AB18	input data from ADC
18	INA11	164	INA11	-	35	EG_P14	AA18	input data from ADC
19	INA12	162	INA12	-	37	EG_P15	AA19	input data from ADC
20	INA13	161	INA13	-	39	EG_P16	Y19	input data from ADC
21	INA14	160	INA14	-	41	EG_P17	AB20	input data from ADC
22	INA15	159	INA15	-	43	EG_P18	Y20	input data from ADC
23	LTC2208_122MHz	152	ADC_CLKA	-	7	EG_P2	V15	buffered clock from ADC
24	OVERFLOW	146	OVFLA	-	49	EG_P21	AB21	overflow input from ADC
25	RAND	145	RAND	-	47	EG_P20	AB22	random enable to ADC
26	PGA	143	PGA	-	51	EG_P22	AA22	PGA enable to ADC
27	DITH	189	DITHER	-	56	EG_P55	V18	dither enable to ADC
28	SHDN	194	-	-	-	-	-	shutdown output to ADC
29	DAC_ALC	137	-	DAC_ALC	16	EG_P39	N6	DAC PWN output level
30	DACD0	195	-	DACD0	50	EG_P53	U16	output data to DAC
31	DACD1	196	-	DACD1	48	EG_P52	U15	output data to DAC
32	DACD2	197	-	DACD2	46	EG_P51	V16	output data to DAC
33	DACD3	200	-	DACD3	42	EG_P50	V14	output data to DAC
34	DACD4	201	-	DACD4	40	EG_P49	T14	output data to DAC
35	DACD5	202	-	DACD5	38	EG_P48	T13	output data to DAC
36	DACD6	203	-	DACD6	36	EG_P47	T12	output data to DAC
37	DACD7	207	-	DACD7	34	EG_P46	R14	output data to DAC
38	DACD8	214	-	DACD8	30	EG_P45	P14	output data to DAC
39	DACD9	216	-	DACD9	28	EG_P44	T8	output data to DAC
40	DACD10	217	-	DACD10	26	EG_P43	T7	output data to DAC
41	DACD11	218	-	DACD11	24	EG_P42	R6	output data to DAC
42	DACD12	219	-	DACD12	20	EG_P41	R5	output data to DAC

43	DACD13	221	-	DACD13	18	EG_P40	P6	output data to DAC
44	CBCLK	240	CBCLK	CBCLK	59	EG_P25	W22	output to CODEC
45	CLRCIN	236	CLRCIN	CLRCIN	61	EG_P26	W21	output to CODEC
46	CLRCOUT	232	CLRCOUT	CLRCOUT	63	EG_P27	V21	output to CODEC
47	CDIN	239	CDIN	CDIN	55	EG_P23	Y22	output to CODEC
48	CMCLK	223	CMCLK	CMCLK	52	EG_P54	U17	master clock to TLV320 audio CODEC
49	CMODE	230	-	-	-	-	-	mode select output to CODEC (I2C or SPI)
50	nCS	231	PH_CODEC_nCS	-	60	EG_P57	V19	chip select output to CODEC
51	nCS	231	-	MIC_CODEC_nCS	57	EG_P24	Y21	
52	MOSI	226	SPI_DATA	SPI_DATA	62*	EG_P58	V20	SPI data output to CODEC
53	SSCK	224	SPI_CLK	SPI_CLK	64*	EG_P59	U20	SPI clock output to CODEC
54	CDOUT	235	-	MIC_CDOUT	45	EG_P19	AA20	mic data input from CODEC
55	PHY_TX0	50	-	-	-	ENET_TXD0	M21	transmit data output to PHY
56	PHY_TX1	49	-	-	-	ENET_TXD1	M20	transmit data output to PHY
57	PHY_TX2	45	-	-	-	ENET_TXD2	N21	transmit data output to PHY
58	PHY_TX3	44	-	-	-	ENET_TXD3	N20	transmit data output to PHY
59	PHY_TX_EN	41	-	-	-	ENET_TXEN	K22	transmit enable output to PHY
60	PHY_TX_CLOCK	43	-	-	-	ENET_GTX_CLK	L22	transmit clock output to PHY
61	PHY_RX0	6	-	-	-	ENET_RXD0	AB6	receive data input from PHY
62	PHY_RX1	13	-	-	-	ENET_RXD1	AB5	receive data input from PHY
63	PHY_RX2	18	-	-	-	ENET_RXD2	AA7	receive data input from PHY
64	PHY_RX3	21	-	-	-	ENET_RXD3	AB7	receive data input from PHY
65	RX_DV	113	-	-	-	ENET_RX_DV	V9	receive data valid input from PHY
66	PHY_RX_CLOCK	31	-	-	-	ENET_RX_CLK	M8	receive data clock input from PHY
67	PHY_CLK125	149	-	-	-	-		125MHz clock input from PHY PLL
68	PHY_INT_N	55	-	-	-	ENET_INTn	N8	interrupt input from PHY
69	PHY_RESET_N	56	-	-	-	ENET_RSTn	K21	reset output to PHY
70	CLK_25MHZ	33	-	-	-	-	-	25MHz clock input from PHY oscillator
71	PHY_MDIO	52	-	-	-	ENET_MDIO	AB12	MDIO data to/from PHY
72	PHY_MDC	51	-	-	-	ENET_MDC	V13	MDIO clock to PHY
73	SCK	68	-	-	-	-	-	clock output to MAC eeprom
74	SI	38	-	-	-	-	-	data output to MAC eeprom SI pin
75	SO	70	-	-	-	-	-	data input from MAC eeprom SO pin
76	CS	87	-	-	-	-	-	chip select output to MAC eeprom
77	NCONFIG	63	-	-	-	RECONF	G6	reload FPGA from config prom when high
78	ADCMOSI	78	-	-	-	-	-	data output to serial ADC
79	ADCCLK	82	-	-	-	-	-	clock output to serial ADC
80	ADCMISO	57	-	-	-	-	-	data input from serial ADC
81	nADCCS	118	-	-	-	-	-	chip select output to serial ADC
82	SPI_SDO	81	-	-	-	-	-	SPI data output to Alex/Apollo

83	SPI_SCK	83	-	-	-	-	-	SPI clock output to Alex/Apollo
84	J15_5	114	-	-	-	-	-	SPI RX data load stobe output to Alex or Apollo enable
85	J15_6	117	-	-	-	-	-	SPI TX data load strobe output to Alex or Apollo reset_n
86	PTT	98	-	FPGA_PTT_N	8	EG_P36	P9	active-low PTT input
87	KEY_DOT	76	-	FPGA_DOT_N	78	EXP_PRESENT	P19	active-low dot input from J6
88	KEY_DASH	73	-	FPGA_DASH_N	58	EG_P56	W19	active-low dash input from J6
89	FPGA_PTT	84	-	PA_KEY	14	EG_P38	M6	active-high PTT output to J11 and J16
90	MODE2	110	-	-	-	DIP_SW4	E16	input: jumper is on Hermes J13 when low
91	ANT_TUNE	94	-	-	-	-	-	input from ATU
92	IO1	95	-	-	-	-	-	active-high output to mute audio amp
93	IO2	46	-	-	-	-	-	PTT input from Apollo
94	IO4	88	-	-	-	-	-	aux digital input from J16
95	IO5	99	-	-	-	-	-	aux digital input from J16
96	IO6	100	-	-	-	-	-	aux digital input from J16
97	IO8	126	-	-	-	-	-	aux digital input from J16
98	USEROUT0	135	-	-	-	-	-	aux open-collector digital outputs to J16
99	USEROUT1	134	-	-	-	-	-	aux open-collector digital outputs to J16
100	USEROUT2	133	-	-	-	-	-	aux open-collector digital outputs to J16
101	USEROUT3	132	-	-	-	-	-	aux open-collector digital outputs to J16
102	USEROUT4	131	-	-	-	-	-	aux open-collector digital outputs to J16
103	USEROUT5	128	-	-	-	-	-	aux open-collector digital outputs to J16
104	USEROUT6	127	-	-	-	-	-	aux open-collector digital outputs to J16
105	Status_LED	80	-	-	-	-	-	active-high configured LED output
106	DEBUG_LED1	9	-	-	-	USER_LED1	B17	active-low user/debug LED output
107	DEBUG_LED2	93	-	-	-	USER_LED2	E19	active-low user/debug LED output
108	DEBUG_LED3	142	-	-	-	USER_LED3	E21	active-low user/debug LED output
109	DEBUG_LED4	139	-	-	-	USER_LED4	B21	active-low user/debug LED output
110	DEBUG_LED5	188	-	-	-	USER_LED5	C20	active-low user/debug LED output
111	DEBUG_LED6	37	-	-	-	USER_LED6	C21	active-low user/debug LED output
112	DEBUG_LED7	111	-	-	-	USER_LED7	D19	active-low user/debug LED output
113	DEBUG_LED8	112	-	-	-	USER_LED8	D21	active-low user/debug LED output
114	DEBUG_LED9	103	-	-	-	-	-	active-low user/debug LED output
115	DEBUG_LED10	106	-	-	-	-	-	active-low user/debug LED output
116	-	-	DRV_CLK_OUT_N	-	67	EG_P29	U21	output to HF2: drive 122.88MHZ to J1 pin 5
117	-	-	-	DAC_CLK	3	RESET_EXPn	U13	output to TX2: clock to DAC
118	-	-	-	EN_RX_ANT	12	EG_P37	M7	output to TX2: t/r switch
119	-	-	-	-	-	DDR3_CLK_50MHZ	H13	input from 50MHZ oscillator
120	-	-	-	-	-	CLK_24MHZ	M9	input from 24MHZ oscillator
Index	**Hermes name**	**Hermes C3 FPGA pin**	**HF2 Name**	**TX2 Name**	**CVA9 J2 pin**	**CVA9 name**	**CVA9 CV FPGA pin**	**Description**

* pins 62 and 64 are shared pins on CVA9